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### Multi-port RAM having means for providing selectable interrupt ...

Multi-port RAM 3 includes an interrupt circuit 4 having an interrupt mode/status register 7 for selecting the specific address to generate interrupts and ...

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devices, and a multi-port random access memory (RAM) used by all of said .... 4120048, Memory with simultaneous sequential and random address modes ...

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### CMOS multiport general purpose register - - US Patent 4737933

each port being addressed by an independent addressing circuit. The ... et al. 4120048, Memory with simultaneous sequential and random address modes ...

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### Low power bank-based multi-port SRAM design due to bank standby ...

The proposed hierarchical concept uses address-decoded .... power bank-based multi-port SRAM design method with. bank standby mode has been proposed in this ...

[ieeexplore.ieee.org/iel5/9366/29746/01354054.pdf](http://ieeexplore.ieee.org/iel5/9366/29746/01354054.pdf) - Similar pages -  
by Z Zhu - 2004 - Related articles - All 2 versions

### MULTI- PORT MEMORY DEVICE FOR BUFFERING BETWEEN HOSTS AND NON ...

The multi-port memory device of claim 3, wherein in a read operation mode of the external memory, a source address provided from the host is stored in the ...

[www.faqs.org/patents/app/20080285372](http://www.faqs.org/patents/app/20080285372) - 70k - Cached - Similar pages -

### [PDF] Parallel I/O Examples Parallel I/O I/O Port Addressing Modes

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Two Addressing Modes. 1) Immediate Port Address. - Can only be 1 byte. - Can only Address Ports 00h through ffh. 2) Port Address Present in DX ...

[www.ece.msstate.edu/~reese/EE3724/lectures/pario/pario.pdf](http://www.ece.msstate.edu/~reese/EE3724/lectures/pario/pario.pdf) - Similar pages -

### New March Tests for Multiport RAM Devices

an addressing sequence of length  $n(n-1)$  as. Fig. 4. A multiport embedded RAM; bus interface devices equipped with IEEE 1149.1 have been labeled ...

[www.springerlink.com/index/V75G172P82557854.pdf](http://www.springerlink.com/index/V75G172P82557854.pdf) - Similar pages -  
by K Chakraborty - 2000 - Cited by 2 - Related articles - All 4 versions

### [PDF] Implementing Multi-Port Memories in ProASICPLUS Devices

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$b\_raddr \Rightarrow$  <output address bus 8-bits (QPM mode)>,. --.  $b\_rdata \Rightarrow$  <output data bus (variable width)>,. Here is the multi-port memory implementation source ...


[www.actel.com/documents/APA\\_MultiPort\\_AN.pdf](http://www.actel.com/documents/APA_MultiPort_AN.pdf) - Similar pages -



### [PDF] Multi-Port AHB SDR/DDR SDRAM Memory Controller BA312



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Oct 13, 2008 ... Programmable row and column address bit widths up to: ... Supports Auto Refresh mode, Self Refresh mode and power-down mode. ...

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The 70V5389 is a 1 Mbit synchronous multi-port SRAM device based on a true FourPort™ architecture, permitting simultaneous access of the same address by up ...

[ftp://ftp.efo.ru/pub/ldt/ldt\\_obzor\\_manypor.ppt](ftp://ftp.efo.ru/pub/ldt/ldt_obzor_manypor.ppt) - Similar pages - 

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